2123

PATENT
068167.0105

Pursuant to 37 C.F.R. § 1.8, I hereby certify that I have information and a reasonable basis for belief that this correspondence will be deposited as first-class mail with the United States Postal Service in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on March 27, 2002.

Signature

3-27-02
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
	§	
Traut, Eric P.	§	Group No.: 2123
	§	
Serial No.: 09/747,492	§	Examiner: Not Yet Assigned
	§	
Filed: December 21, 2000	§	
	§	
Invention: System and Method for the Logical Substitution of Processor Control in an Emulated Computing Environment	§	

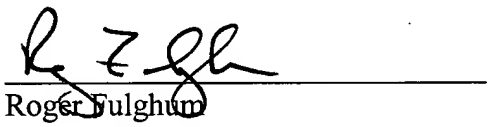
Commissioner for Patents
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Applicant respectfully requests, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner. Pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

The information disclosure statement submitted herewith is being submitted before the mailing of the first office action on the merits. Applicants believe that no fee is required. If a fee is required, please charge any fee to Deposit Account No. 02-0383 of Baker Botts L.L.P.

Respectfully submitted,



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Date: March 27, 2002

PTO-1449

Information Disclosure Citation in an Application

Application No.	Applicant(s)		
09/747,492	Eric P. Traut		
Docket Number	Group Art Unit	Filing Date	
068167.0105	2123	12/21/00	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A	5,815,686	9/29/98	Earl, et al.	395	500	9/12/96
	B	4,779,188	10/18/88	Gum et al.	364	200	10/19/87

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	C	EP 0 645 701 A2	26/09/94	EPO	G06F	9/455	X	

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	
	D	PCT International Search Report in International Application No. PCT/US 01/22276, International filing date 16/07/01, mail date 07/03/02.	
	E	Traut E, "Building the Virtual PC," *Byte*, McGraw-Hill Inc., Vol. 22, No. 11, pp. 51-52, 1 November 1997.	
	F	"Intel386 DX Microprocessor," *Intel*, pp. 32-58, 31 December 1995.	
	G	"MacIntosh and Technology: Changing Chips in the Middle of the Stream, or Apple Takes a Risc," URL:www.btech.co/changingchips.html, paragraphs '0006!-'0007!, retrieved 12/10/01.	
	H	"M68040 User's Manual," Motorola, Inc., Chapter 3, copyright 1990, revised 1992, 1993.	
	I	Osisek DL et al., "ESA/390 Interpretive-Execution Architecture, Foundation for VM/ESA," *IBM Systems Journal*, Vol. 30, No. 1, pp. 34-51, 1991.	
	J	Shang Rong Tsai et al., On the Architectural Support for Logical Machine Systems," *Microprocessing and Microprogramming*, Vol. 22, No. 2, pp. 81-96, February 1988.	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.